Sheet	1	of	1
-------	---	----	---

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMEN  UNDER 37 CFR 1.97						ATTY. DOCKET NO. SER PD030014				IAL NO.		
					ENT	APPLICANTS Jens Peter Wittenburg et al.						
		(Use several	sheets if	necessary)		FILING Herewi			GROU	ı₽ .		
				U.S. PATENT	DOCUMENT	TS						
EXAMINE INITIAL		DOCUMENT NUMBER	ISSUE DATE	APPLICANT/P.	ATENTEE		CLASS	SUB- CLASS	FILING I			
AL	AA	5,185,868	2/9/93	Tran								
	AB											
	AC				<u> </u>		-	· ·				
	AD								-			
	AE					<u> </u>						
	AF			<del> </del>								
}	AG											
	AH				·	<del></del>						
		.I	<u> </u>	FOREIGN PATE	TT DOCUME	:NTS						
		DOCUMENT NUMBER	PUBL. DATE	COUNTRY			CLASS	SUB- CLASS	TRANS	ELATION No		
AL	AI	0039669	7/6/00	PCT	· · · · · · · · · · · · · · · · · · ·				1	T		
	AJ											
	AK	•										
	AL											
	AM				· · · · · · · · · · · · · · · · · · ·	w.				<del>                                     </del>		
	AN											
отн	ER IN	FORMATION (Ir	cluding A	thor, Title,	Pub.Date	e, Perti	nent Pa	ages. Co	Juntry.	Etc.)		
AL	AO	Yoshida a Microp Computer	MATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.) Yoshida et al, "A Strategy for Avoiding Pipeline Interlock Delays in a Microprocessor", Proceedings of the International Conference on Computer Design: VLSI in Computers and Processors, September 17-19									
AL	AP	Search F	990, pages 14-19 earch Report for EP Appln. No. 03090089 dated July 31, 2003									
	AQ											
EXAMINE	I R			Т	DATE CONS	SIDERED						
/Aimee Li/						09/28/2006						
SUBMITT	ED BY	: 10.	( /			<del>-</del>		· .				
Rei	tsena	Lin A		- REG. NO.:	42.804		DATE	· March	20 20	10.4		